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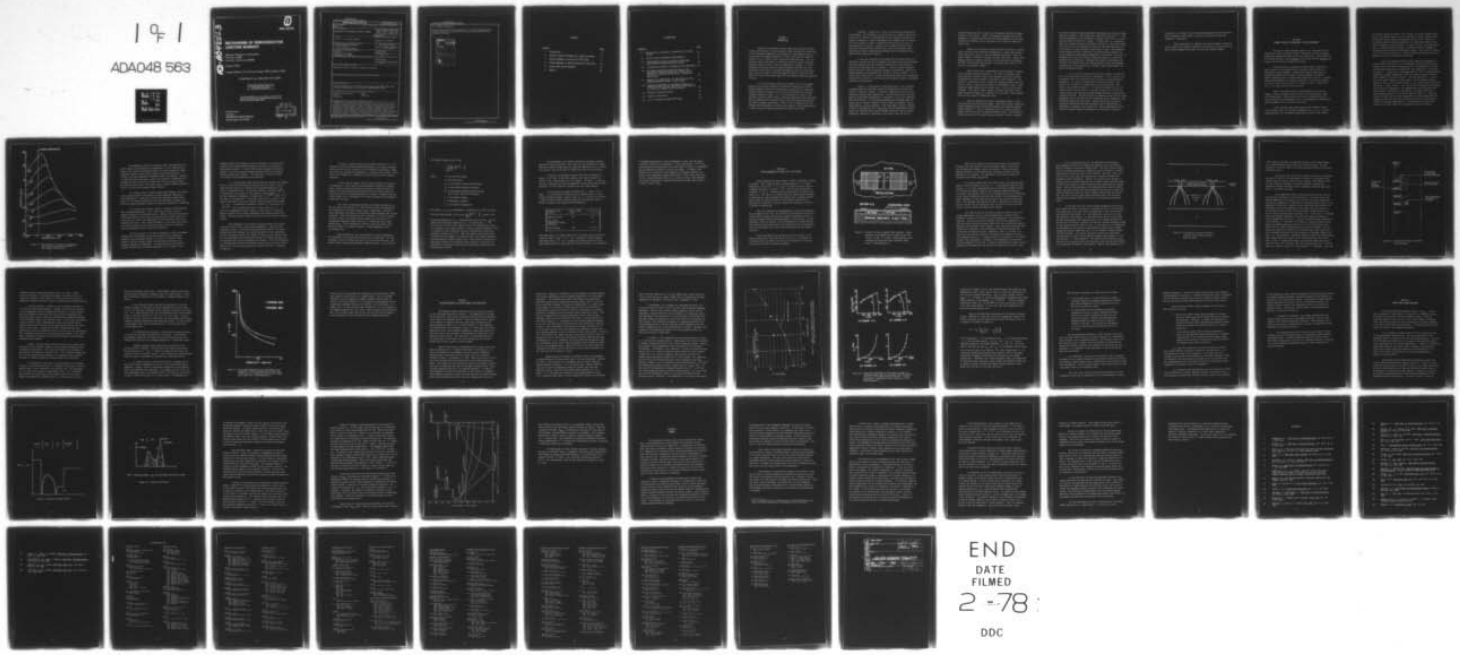

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MECHANISMS OF SEMICONDUCTOR JUNCTION BURNOUT

Mission Research Corporation
P.O. Box 1209
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August 1976

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Mechanisms of semiconductor junction burnout are reviewed with particular emphasis on parameters controlling variation in energy to achieve second breakdown and device damage. Stabilizing effects promoting uniform current distribution and destabilizing effects promoting filamentary currents are identified. Those destabilizing factors involving thermal changes lead to thermal-mode second breakdown. They include the resistivity peak and reverse saturation current. A nonthermal destabilizing effect at high injection conditions leads to current-mode second breakdown. The dominant mode depends

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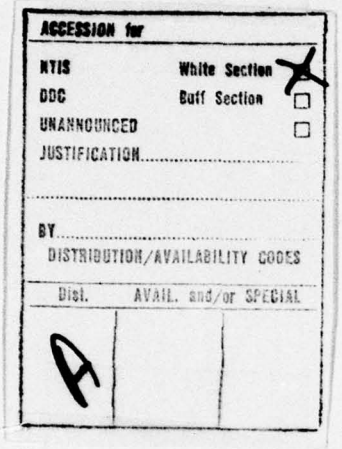
on device parameters and the current level. A minimum energy needed to achieve damage can be estimated for each destabilizing mechanism from mechanisms knowledge.



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SECTION 1
INTRODUCTION

Designers of electronic systems subjected to pulsed electrical stresses need criteria for safe operation (high confidence that there will be no unacceptable degradation of parameters) of semiconductor devices. It is known that the damage thresholds of similar units may vary widely (a spread of up to a factor of ten in energy has been observed). It is important to know at what level to limit the electrical stress on typical electronic parts to assure a very low probability of damage. It is also important to identify screens or process controls that will raise the acceptable stress level, or increase confidence in survival of the parts. Also, rules are needed by which the damage threshold is scaled for different electrical stress pulse shapes and for combined electrical-radiation stresses.

It is not possible to achieve the needed levels of low damage probability with high confidence by statistical testing alone without making assumptions about the extrapolation of sample data to large populations, because the sample sizes for low failure probability and high confidence become too large. It is also not possible to apply a fully realistic electrical pulse screen to eliminate potentially weak individuals from the population of available devices, since electrical-pulse screens are known to degrade some devices. There is also no adequate basis for assuming that the population of devices that passes a given screening test is better than the original population that entered the screen.

Therefore, a sample test, screen, or alternative procedure must be determined. The alternative can take the form of a process control (ensuring that all devices as manufactured maintain acceptable uniformity of relevant parameters). Quality conformance tests (sample tests) are effective when a method is known to extrapolate the results of the test to a large population of devices. Screens (tests through which each device must pass) are particularly valuable when a causal relationship can be established between a nondegrading measurement and the subsequent device behavior under operational stresses.

In any case, knowledge of the mechanisms of junction burnout is required to identify the device parameters that effect the burnout threshold. From this knowledge and data concerning variations of these parameters, the worst-case threshold can be estimated. A subset of these parameters, whose variations in normal production produce an unacceptable variation in burnout threshold, are candidates for screens or process controls. It is likely that in many devices a useful safe operating regime can be prescribed without process controls or tests beyond those normally applied to establish the device's functionality.

There is a large amount of experimental data in the literature on damage thresholds and failure modes for semiconductor junctions subjected to electrical stresses. In addition, numerous theories have been advanced to explain these observations. At first glance, these data and theories often appear contradictory, inconsistent, or at least confusing. More often than not, the individual experiments are performed under conditions that are widely different from one another in geometry, device, doping density, and pulse duration. Each investigator naturally advances a theory or explanation that is consistent with his experimental results. Much of the confusion about second breakdown apparently arises from the assumption, conscious or unconscious, that there is only one kind of

junction burnout and that a single set of phenomena controls the damage processes in all devices. There is considerable evidence that such an assumption is erroneous and that the controlling parameters may be quite different for different device structures, pulse widths and forward or reverse bias.

Studies of the effects of pulsed electrical stresses on semiconductor junction devices have been performed with a large range of pulse widths (few nsec to many sec) and corresponding amplitudes. Since one form of damage is related to heating, the power necessary to achieve this damage (voltage and current) increases as the pulse width is shortened. For TREE, EMP, and SGEMP applications, the shorter pulse widths (.01-10 nsec) are of principal interest.

Under reverse bias a semiconductor junction appears to undergo three reasonably distinct transitions. The first is breakdown, which occurs when the electrical field at the junction exceeds the threshold for generation of free carriers by avalanche or Zener mechanisms. The second is a transition to lower voltage (at constant current), which may occur as soon as a high level of current is established or after a delay time whose length depends on the current level. This is called second breakdown. The third is another change in voltage associated with permanent structural damage (e.g., melting) in the junction. Under forward bias only the latter two transitions occur.

There are apparently two types of permanent effects: those associated with surface and bulk damage. Some devices exhibit significant surface degradation after junction avalanching, even without incurring second breakdown.[1,2] This is presumably due to hot carriers becoming trapped in the oxide layer or forming interface states. This effect has serious implications for pulsed electrical methods of device screening.

All devices eventually undergo permanent bulk damage when electrical energy deposition produces a large enough local temperature excursion. [3, 4] The critical temperature may be determined by melting (1420°C in Si) or by enhanced diffusion and drift of a dopant. In either case, it is generally true that a thermal-electrical instability develops at a much lower temperature, which allows the subsequent current flow and energy deposition to be localized in a small fraction of the device's volume. The dependence of any thermal-electrical instability on electrical pulse length is obviously affected by the geometry (dimensions) of the device, insofar as it determines heat flow from regions of high power density to cooler bulk semiconductor and substrate. Phenomena that compete in determining the junction's net thermal-electrical characteristics include the dependence on temperature of bulk resistivity, avalanche field, Zener voltage, and reverse saturation current.

In this review of semiconductor junction burnout, the multiplicity of failure mechanisms and modes is emphasized. Various theories and experimental data are reviewed for their relevance to second breakdown and damage. The instability mechanisms mentioned by different investigators are discussed as probable causes of second breakdown. The work by three different authors[5,6,7] on second breakdown in silicon-on-sapphire (SOS) diode structures is reviewed, because their results give a particularly clear picture of certain thermal processes in pulsed semiconductor junctions. The physics that are dominant in these SOS structures undoubtedly also are present in more conventional device geometries, such as diffused diodes and transistors. The main uncertainty is how the conclusions derived from the SOS experiments must be modified due to differences in geometry, heat sinking, etc. These uncertainties and results for diffused diodes and transistors are discussed in Section 4.

In Section 5, a different class of failure mechanisms (called current-mode second breakdown), which usually occurs only in epitaxial diodes and transistors is described.

These discussions will emphasize the second breakdown transition and the factors that appear to determine the variation of energy deposition up to second breakdown and between its onset and permanent damage.

SECTION 2
THERMAL INSTABILITY MECHANISMS IN SECOND BREAKDOWN

The onset of second breakdown appears to be associated with an instability in which the current tends to concentrate in small filaments rather than spreading uniformly across the junction area. Such instability will develop whenever a local increase in the current density decreases the electric field required to sustain the current.

Various theories are proposed to explain these instabilities. These theories can be grouped into two categories, thermal-mode and current-mode second breakdown. Thermal-mode breakdown means that the triggering mechanism for the onset of second breakdown is primarily thermal (requiring time to achieve energy deposition); whereas, in current-mode second breakdown it is primarily electrical, and can occur promptly. In both cases the ultimate failure of the device is due to thermal run-away, if the high current condition persists.

Some of the confusion about second breakdown is due to the number of theories proposed, some of which are very similar but stated in different words. These theories will now be reviewed briefly and their similarities and differences noted. The mechanisms of thermal-mode second breakdown will be discussed in Section 5.

Terms associated with thermal-mode second breakdown include: (1) resistivity peak, (2) intrinsic temperature, (3) $n_i > N_D$, (4) avalanche quenching, (5) recombination-generation current = total current,

(6) reverse saturation current = total current, (7) lateral thermal instability, (8) thermal runaway, and (9) local melt. Actually, there are only two distinct thermal-instability mechanisms in this list: namely, the resistivity peak and avalanche quenching. The other seven items are just other descriptions of these effects, or results of them. Avalanche quenching is a junction property; whereas, the resistivity peak is primarily associated with the neutrally-charged bulk region. Thus, these two effects are in the series in the device. Either instability might occur first, depending on the device and the test conditions.

Due to the competing effects of the temperature dependences of carrier mobility and density in a semiconductor, the bulk resistivity (ρ) reaches a peak after first increasing from its room temperature value and then decreases approximately exponentially with temperature. The initial increase in ρ results from a decreasing mobility, due to increased phonon scattering at higher temperatures, while the carrier density is approximately constant in extrinsic material. The final decrease in ρ occurs due to the rapid increase in carrier density when the material becomes intrinsic; that is, the intrinsic density n_i is greater than the extrinsic doping N_D . Thus, items (1), (2), and (3) above correspond to essentially the same critical temperature. The temperature at the resistivity peak varies with the resistivity of the material. Resistivity curves for various doping densities in silicon are shown in Figure 2.1. Since the resistivity peak occurs at lower temperatures for lower doping densities (higher resistivities) and since the higher resistivity regions heat up faster for the same current density, the high-resistivity side of the junction is the most sensitive to the peak-resistivity instability.

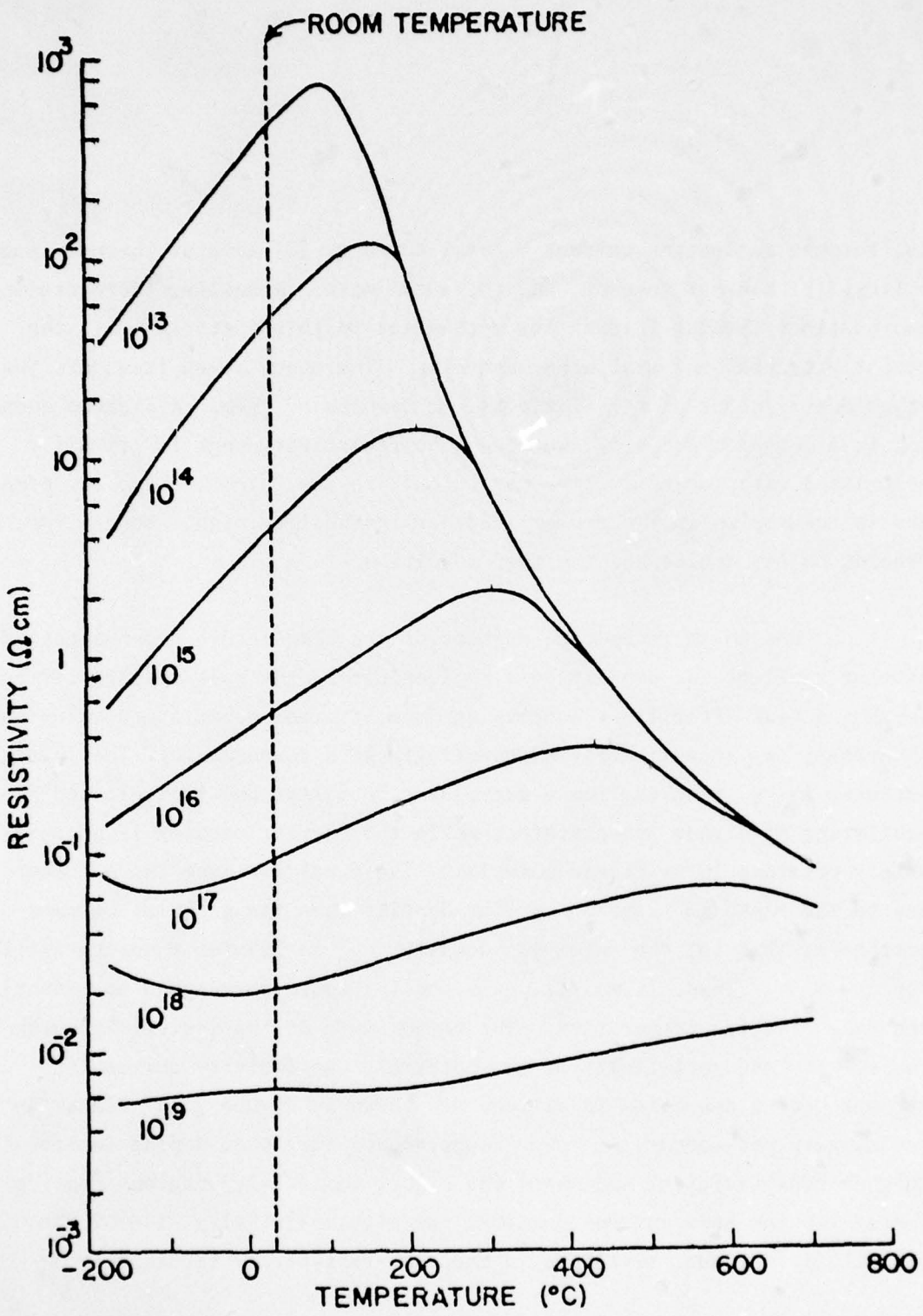


Figure 2.1 Resistivity as a function of temperature for n-type silicon (from Reference 7; after Runyan, Reference 8).

At temperatures below the resistivity peak, the bulk material is stable against local fluctuations in temperature. As the temperature increases, the increased resistivity reduces the current through the higher-temperature region so that the heat input to that region decreases. As a result, the local temperature fluctuation tends to be reduced. Conversely, above the resistivity peak, a small local increase in temperature will decrease the local resistivity and cause more current to funnel through the initially hotter spot. This effect causes a lateral thermal instability (Item 7) and can lead to thermal runaway (Item 8).

In a junction that is reverse-biased above breakdown, the current can be produced either by avalanching or Zener tunneling, depending on the doping density. Junctions in silicon with breakdown voltages below about 6V are usually controlled by the true Zener effect, whereas junctions with larger breakdown voltages are invariably dominated by avalanching.

It is known that the Zener voltage at constant current decreases with increasing temperature. Thus, a true Zener junction is always thermally unstable in the junction region. However, the stabilizing effect of the bulk region in series with the junction allows stable operation of Zener devices as long as the temperature for the resistivity peak is not exceeded in the bulk. Thus, second breakdown in a pure Zener diode should be controlled entirely by the resistivity peak in the bulk, although we have no experimental data to verify this conclusion.

On the other hand, it is known experimentally that the breakdown voltage for an avalanching silicon device increases with temperature. Therefore, the avalanching condition, by itself, is thermally stable. However, the total current through a reverse-biased junction is only partially supplied by avalanching. The remainder comes from diffusion current from the bulk, recombination-generation (R-G) current in the

depletion region of the junction, carrier injection to a collector-base junction from a forward-biased emitter-base junction, and ionization-induced photo-currents. If any of these current components become comparable to the total current maintained through the junction, then the avalanche current must decrease. This means that the electric fields which produce the avalanching must also decrease.

In a reverse-biased diode without radiation, the only two currents that will occur are the diffusion current and the R-G current. Both of these currents increase very rapidly with increasing temperature, but usually at different rates. The diffusion current in extrinsic material is proportional to the square of the intrinsic carrier density n_i^2, so its main temperature dependence is proportional to $e^{-E_G/KT}$ where E_G is the width of the energy gap. On the other hand, the R-G current is dominated by deep defect levels with energies from the nearest band of about $E_d = E_G/2$. Its temperature dependence, therefore, is proportional to $e^{-E_G/2\,kT}$. The pre-exponential factor is much larger for n_i^2, so that at low temperatures the R-G current is larger (due to the smaller negative exponent) and at higher temperatures the diffusion current dominates. These two currents combine to make up the total reverse-saturation current.

Both components of the reverse saturation current are destabilizing since they increase with increasing temperature. When the local temperature reaches a point where the destabilizing effect of the reverse saturation current overpowers the stabilizing effects of the avalanching process, the current density will increase in this hot spot causing a higher local temperature, the destabilizing current will further increase, and the junction field and the avalanching will decrease. Thus, the avalanching is "quenched" when the reverse saturation current equals the total current. Items (4) and (6) are thus basically the same, and item (5) is contained in item (6).

If there is current injection from another junction (i.e., in a transistor) and/or radiation-induced photocurrents, the reverse saturation current does not have to increase as far to quench the avalanching. Therefore, the local destabilizing temperature is reduced, and the energy threshold for this instability is reduced by carrier injection and/or ionizing radiation.

In the local melt theory (Item 9), the instability is assumed to be triggered by a local region of the semiconductor reaching its melting point, causing a metallic-like molten region with a reduced resistivity. However, the avalanche-quenching discussed above will always produce an instability before the melting temperature is reached. Therefore, melting is more likely to be a consequence of a current instability and channeling rather than its cause.

Thus, there are general mechanisms for thermal instabilities in the bulk and at the junction, i.e., the resistivity peak and quenching of the avalanching by some other current source, respectively. Both mechanisms apparently participate in reverse-bias second breakdown under various conditions. Since the junction and bulk resistance of a diode or transistor are in series, these mechanisms may compete with each other in an intermediate temperature range, where one is stabilizing and the other destabilizing. At low temperatures, both are stabilizing (unless Zener emission controls the junction current); at high temperatures, both are destabilizing.

Under forward bias, the current profile is again determined by the combination of junction and bulk resistivity voltage drops. The bulk resistance is still a stabilizing factor up to the resistivity peak. The diode's forward voltage drop represents competing factors. For a PN diode

with lighter doping on the P side:

$$I = \frac{e\ A\ N_p}{\sqrt{D_n\ \tau_p}} \left(e^{eV/kT} - 1\right)$$

where: e is the electron charge,

A is the diode area,

N_p is the minority carrier concentration,

D_n is the electron diffusion constant,

τ_p is the express minority-carrier lifetime, (all on the P side of the junction)

V is the applied voltage,

k is Boltzmann's constant,

T is the absolute temperature.

The factors $e\ A\ N_p$ are independent of temperature (at least well below the resistivity maximum), the factors $\frac{1}{\sqrt{D_n}} \left(e^{eV/kT} - 1\right)$ increase with increasing temperature (i.e., is destabilizing) and the factor $\frac{1}{\sqrt{\tau_p}}$ decreases with increasing temperature (i.e., is stabilizing). The net result is that at low currents (low V) the current density tends to be uniform, but at higher currents it tends to become filamentary. This is a problem in power transistor and can be ameliorated by resistively loading the contact area.[9,10,11] With such loading, when current tries to funnel into one filament, the resistive drop at the contact stabilizes the flow pattern to higher current levels. This resistive ballasting is particularly effective in transistor emitter contacts, because the low-resistivity of the emitter region does not provide much protection from a destabilized junction.

The development of the thermal instabilities depends on energy deposition and heat diffusion. Thus, there are two characteristic times; the time to deposit enough energy to bring the temperature up to a critical value and the time for the heat to diffuse away from its source region.

In silicon, the threshold electric field for avalanching is around 2×10^5 V/cm. Using a heat capacity for silicon of about 1.6 J/cm^3-C° and a current density of, for example, 10^4 A/cm^2, a time of 240 nsec is required to raise the temperature of the junction region 300°C. Obviously, this time decreases inversely with the current density.

The characteristic thermal diffusion time τ equals L^2/D, where L is the distance that the heat has to diffuse, and D is the thermal diffusion constant. Using a value of $D = 1$ cm^2/sec for silicon, a table of characteristic diffusion times can be constructed based on typical low-power, high-frequency device dimensions.

Characteristic Region	Typical Length L (μm)	$\tau = L^2/D$ (sec)
Depletion width	0.3	10^{-9}
Base width; Epitaxial collector thickness	3	10^{-7}
Chip thickness	200	$4 \times I0^{-4}$

This table means, for example, that heat will diffuse across the base or epitaxial width 3 (μm) in 10^{-7} sec. Therefore, for pulse lengths much greater than 10^{-7} sec, a steady state thermal profile will have been established across these regions by thermal diffusion, the temperature

is primarily proportional to power independent of time, and the effects of the heat sinks must be considered. At very short pulses ($\sim 10^{-9}$ sec), the heat cannot flow appreciably out of the region in which it is generated, and the temperature increases linearly with energy. In between, heat generation in the depletion layer competes with thermal diffusion, producing a peak temperature roughly proportional to power times square root of time. Larger-dimension devices (e.g., higher voltage, lower frequency) will exhibit characteristic thermal-diffusion times longer than these by a factor of ten or more.

SECTION 3
SECOND BREAKDOWN IN LATERAL SOS P^+ NN^+ DIODES

Second breakdown has been studied in detail in epitaxial silicon-on-sapphire (SOS) diodes by three different groups.[5,6,7] In these experiments, a thin layer (≃1 to 2 μm) of n-type silicon is grown on a sapphire substrate. A lateral P^+ NN^+ diode is then fabricated by diffusing P^+ and N^+ contacts across the two ends of the device (see Figure 3.1). The devices are studied before and during second breakdown by observing the light (avalanche and thermal) that is emitted from the device during an electrical pulse and the thermal distributions as determined by variations in optical transmission through the silicon as a function of temperature.

There are advantages and disadvantages to this device geometry. The advantages are that the PN junction can be viewed from the side in profile and the spatial distribution of physical parameters can be observed and studied parallel and perpendicular to the junction. The disadvantage is that the geometry is not representative of normal devices. The conclusions from these studies are influenced by the two-dimensional nature of the geometry and by the unique heat sinking to the sapphire substrate.

These experiments have provided such a clear picture of the physical processes in these special devices that it is instructive to review the results in detail, in spite of the limitations in relating the results to devices of practical geometry.

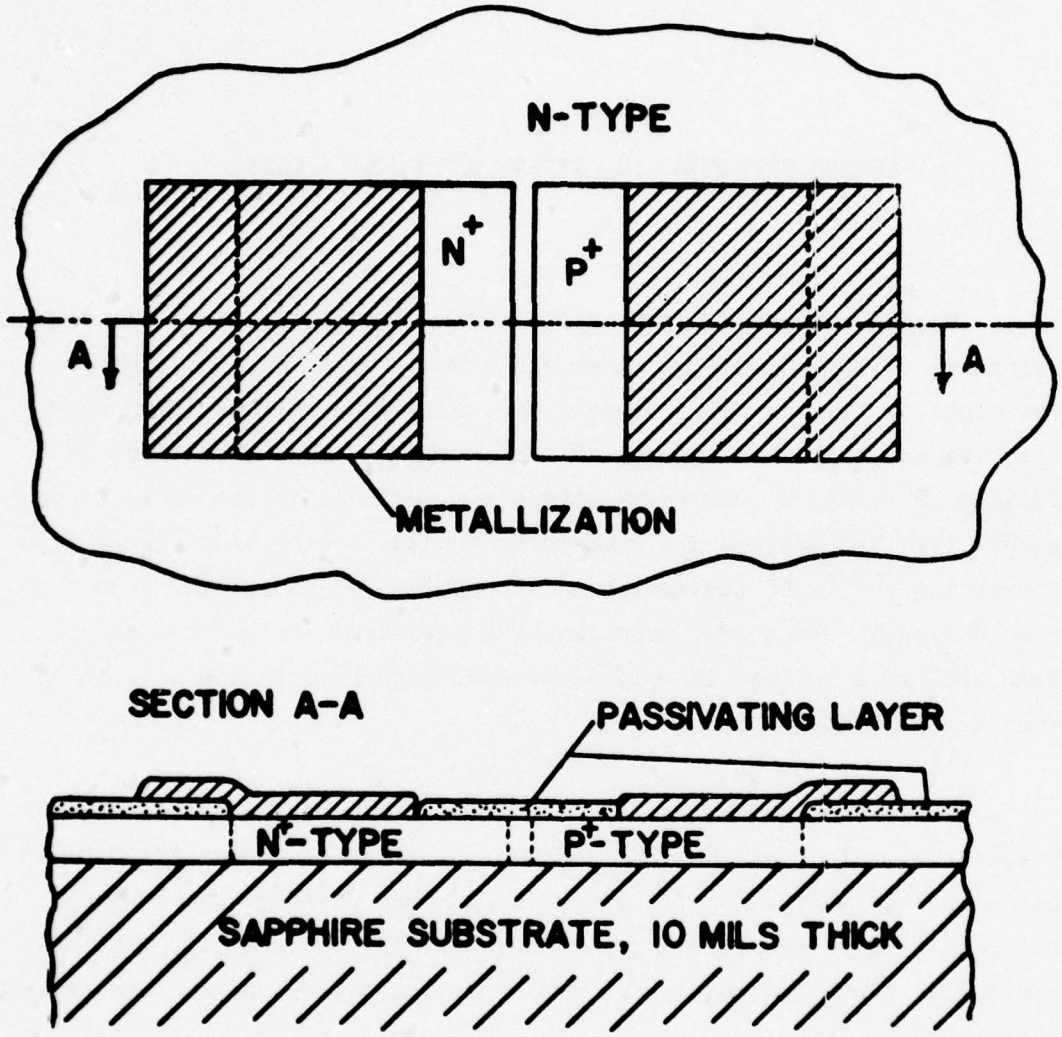


Figure 3.1 Typical silicon-on-sapphire diode geometry. Doping materials are diffused into an n-type silicon film to form P^+ and N^+ regions. Metallizations are of aluminum and passivating layers thermally grown oxide. (From Reference 7)

When the test diodes are reverse-biased barely into avalanche breakdown, the light emission from the avalanche region is confined to thin (microplasma) filaments across the junction. These microplasmas probably nucleate on lattice defects and are purely electronic and non-degrading to the junction. The temperature of the junction remains at essentially the ambient temperature.

At slightly higher biases and current levels, the junction region begins to heat up slightly due to the $E \cdot I$ power-density input near the junction. It is known experimentally that the avalanche breakdown voltage in PN junctions increases slightly with increasing ambient temperature. This effect, when applied locally to an avalanching junction, is stabilizing to the current distribution and causes the current to be distributed more nearly uniformly over the junction area than at the smaller avalanche currents. The avalanche light emission becomes a continuous line coincident with the junction and the temperature near the junction and in the N bulk region is fairly uniform and somwhat above ambient.

This pattern persists to higher voltage and current levels (and average temperatures) until a critical temperature is reached locally. Budenstein[7] observed two different critical temperatures in reverse-biased junctions. The one which usually occurred first was the temperature at which the reverse saturation current density for the reverse-biased junction approached the avalanche current density. Other authors have described this transition as quenching of the avalanching by generation-recombination current from the depletion region. Regardless what it is called, it is clear that an instability started at the junction in Budenstein's devices and propagated across the N region, which had a resistivity of .064 ohm-cm in most of his experiments. Presumably, this propagation was associated with the temperature in the bulk N material approaching the second critical temperature corresponding to the peak of the electrical resistivity curve.

In any avalanching junction, the temperature distribution is never perfectly uniform due to temperature gradients which are formed as the heat diffuses to the various thermal sinks. Thus, the critical temperature for avalanche quenching by a competing source of carriers is normally reached first at some local point in the junction. When this occurs, the local electric field across the junction has to decrease to reduce the avalanche current contribution. However, the resulting local decrease in voltage across the junction decreases the avalanche current generated nearby and allows more current to funnel through the high-temperature low-voltage region. Since the SOS experiments were performed using a constant current source, the excess current that goes through the hot spot had to reduce the current through the junction at points slightly removed from the hot spot. Thus, the core of the hot spots become even hotter due to the increased current and the regions around the hot spot cease avalanching and become cooler.

At the point where the current filament through the junction hot spot reached the bulk N material, the current fans out to try to minimize the voltage drop in the bulk, which is proportional to the current density and resistivity (see Figure 3.2). This fanning out results in a voltage drop parallel to the junction. If the current level and the device width are both large enough, the voltage parallel to the junction measured from the hot spot will allow the junction to reach the avalanche breakdown voltage at some distance from the first hot spot. At that point, it is energetically more favorable for the current to form another hot-spot current filament through the junction rather than for all of the current to funnel through the first filament. For some low resistivity devices with large short current pulses, as many as thirty current filaments were observed in a 21.5 mil wide and 1 μ - thick junction.[7] For high resistivity material, small devices, and low current levels with long pulses, only one spot was observed. It occurred near the middle of the junction. There is not enough room in

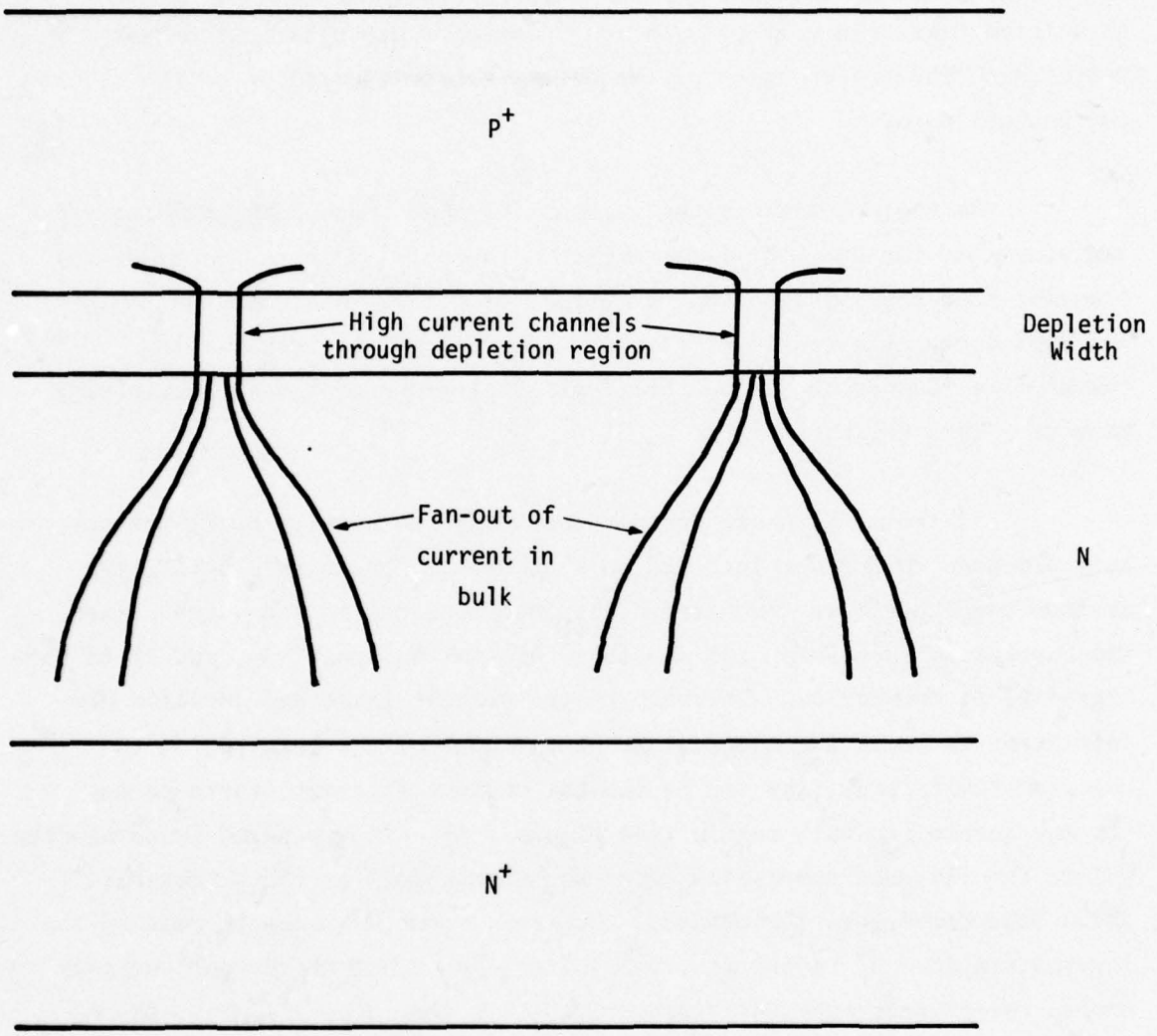


Figure 3.2 Illustration of fan-out of current in diode base after channeling through depletion region.

a small device to develop a voltage drop parallel to the junction equal to a large breakdown voltage with long, low-current pulses. The heat diffuses to the cooler edges of the device making the middle of the device the hottest point.

At the point where the current filament reached the bulk material and starts to fan out, the temperature in the bulk is increased by heat transfer from the junction and by current crowding. What happens to the hot spot during the remainder of the pulse depends on whether this temperature reaches the second critical temperature mentioned previously, that is - the resistivity peak.

If the temperature doesn't reach the resistivity peak, the hot spot proceeds no further into the bulk material. Up to this point, the maximum temperature in the material is less than its melting temperature, the current filamentation is repeatable in time and position, and it is non-degrading to the device. However, if the current level and duration are sufficient to raise the temperature at the edge of the bulk region to the resistivity peak, the tip of the hot current filament starts to eat its way across the bulk region (see Figure 3.3). If the pulse is terminated before the filament completely crosses the bulk region, the process is still nondegrading to the device. However, when the filament reached the low-resistivity N^+ substrate, the voltage (at constant current) quickly drops, the current apparently constricts to a very fine filament, and a molten track is usually formed along the core of the filament. Once the device has cooled and the material has recrystallized, the burnout path is not a permanent low-resistivity path, although it noticeably degrades the diode I-V characteristic. Subsequent high level electrical pulses produce other burnout paths that usually do not coincide with the first failure path. If the N region resistivity is not too much higher than the resistivity of the N^+ substrate, when the filament reaches the N^+ region, there is a relatively large IR drop across the N^+ substrate. Thus, the

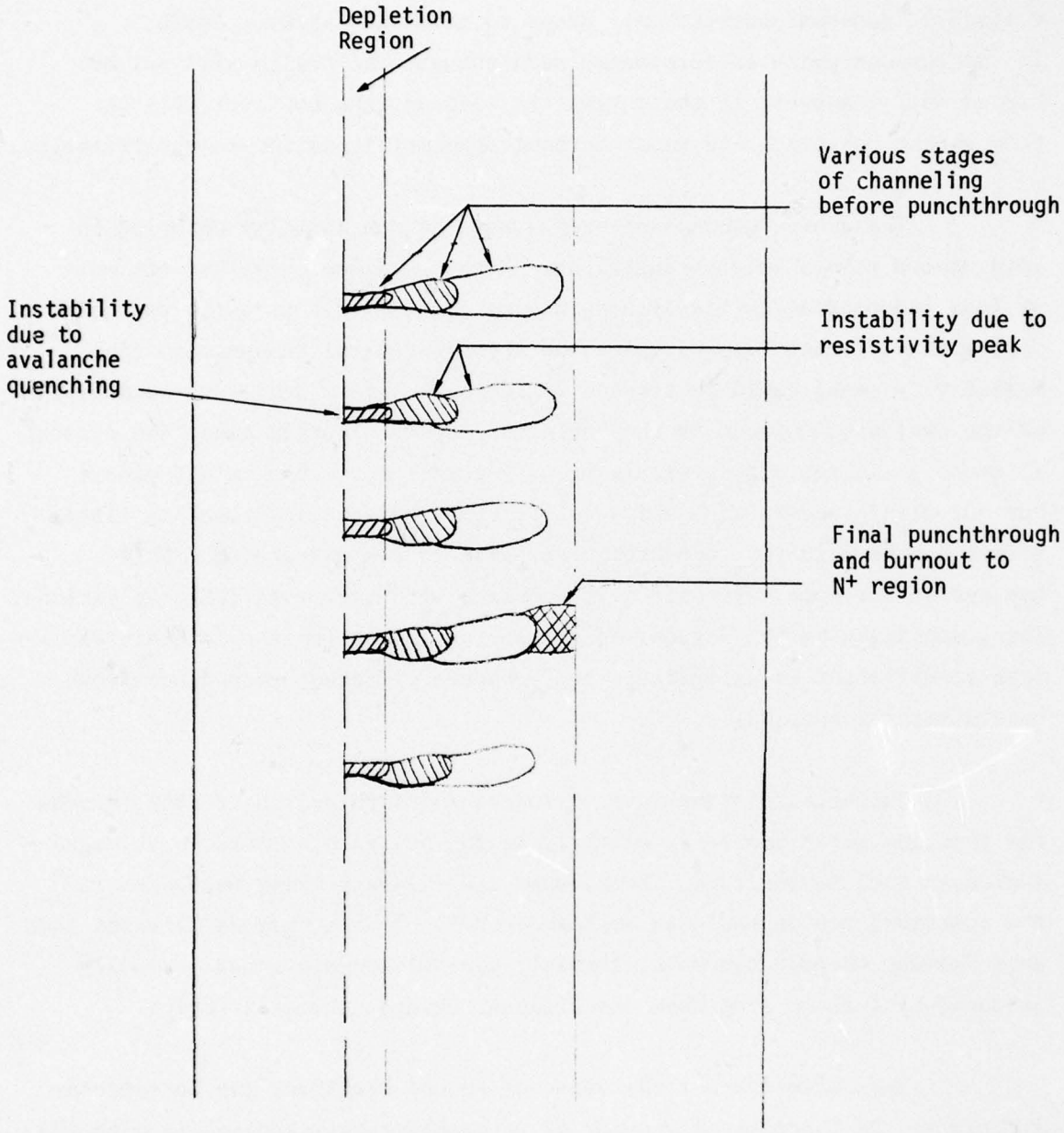


Figure 3.3 Illustration of growth of filaments in SOS experiments.

voltage at constant current only drops to this IR value. Again, if the current pulse is terminated soon enough, the device will not be burned out. However, if the current is left on, the hot spot will eat through the substrate and cause burnout from metallization-to-metallization.

The above sequence of events was the one normally observed in .064 ohm-cm reverse-biased junctions. However, since there are two more or less independent critical temperatures involved; it is quite possible that with different resistivities the second critical temperature (the resistivity peak) could be reached in the bulk before achieving quenching of the avalanche current in the repletion layer. In this case, the current filament nucleates almost simultaneously across the whole bulk region, burnout always occurs with only one hot spot, and the junction has little effect on the results. Budenstein was able to demonstrate this bulk nucleation for some low resistivity devices with very long (DC) excitations. Thus, depending on the device resistivity and pulse lengths in their experiments, different investigators could observe different second breakdown mechanisms and thresholds.

During a constant-current reverse-bias pulse, the voltage across the junction first increases slightly as the avalanche-breakdown voltage increases with temperature. Then, when the filament first nucleates in the junction, the increase in voltage ceases. As the current filament then eats its way through the bulk material, the voltage decreases gradually, followed by a sharp drop when the filament bridges the bulk region.

The definition of the onset of second breakdown can be somewhat arbitrary. On theoretical grounds it is tempting to associate it with the point at which a local instability first develops (e.g., the development of a hot spot at the junction in Budenstein's work). If an experiment only measures the current and voltage through a junction, this point appears in Budenstein's experiments only as a subtle change in slope of

the device resistance versus time. A more dramatic change in resistance occurs when the instability propagates across the lightly doped N layer. But in Budenstein's devices this corresponded to permanent damage to the devices.

One of the main results from the SOS experiments is that the threshold current for the onset of second breakdown with a pulse length of 100 μsec decreases significantly with increased resistivity (see Figure 3.4). For a pulse length of 100 μsec the threshold current varied approximately as the bulk resistivity to the (-3/4) or (-1/2) power. A second result is that for a given bulk resistivity, the pulse length before second breakdown increased considerably with decreasing current. At high currents a large number of hot spots developed quickly. At low currents only a few developed slowly.

For forward-biased junctions, a single hot spot always nucleated in the bulk of the device and burnout was very abrupt. After burnout, the permanent damage from a forward-bias failure was qualitatively and quantitatively similar to the permanent damage due to reverse-bias pulses.

Filament nucleation and burnout were also observed in bulk material without a junction. In these cases, the contacts did not have the low-resistivity P^+ and N^+ regions to smooth out the current concentrations near the metallic contacts. Thus, burnouts were often nucleated where the current concentrated at irregularities around the contacts.

As stated previously, the physics that play a dominant role in these SOS structures undoubtedly also occur in more conventional device geometries. However, there are significant differences in the geometries which could influence their importance. For example, because of the very thin semiconductor sheet, the depletion layer is effectively a line source of power, rather than a plane as in a normal device. The dominant heat

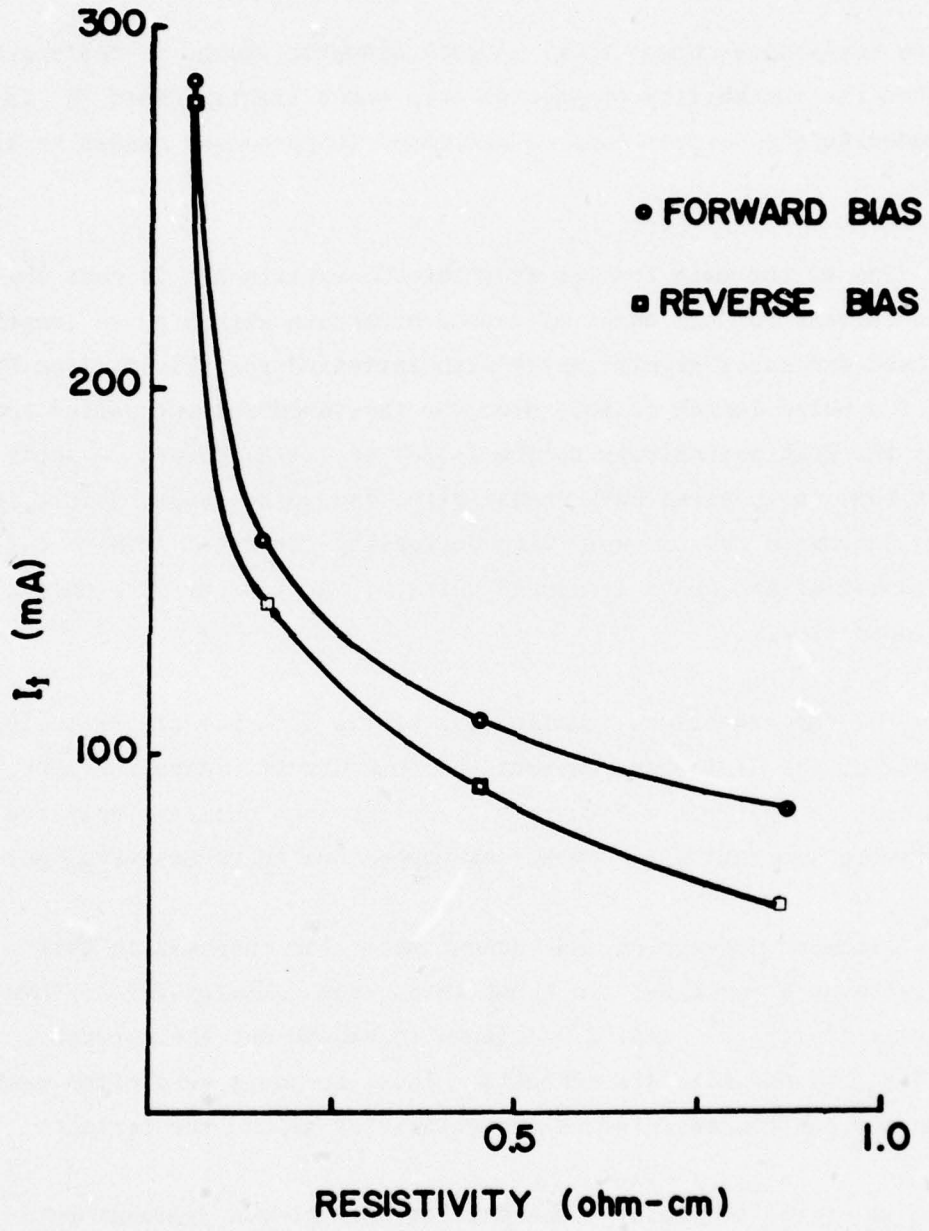


Figure 3.4 The current required to bring the diodes to the threshold of second breakdown with a delay time of 100 μsec as a function of resistivity, forward and reverse bias. (From Reference 7)

flow will be to the substrate and transverse to the current flow, rather than along the current flow as in a normal device. Also, the thermal conductivity of the sapphire is somewhat different from the value in silicon, so the heat transfer from a hot spot in the SOS geometry must be significantly different from the heat transfer in a normal device. For example, for a silicon epitaxial layer thickness of 1 μ, the influence of the sapphire substrate as a heat sink is felt in about 10 nsec (Section 2). Thus, for any times longer than 10 nsec, the heat flow rate and pattern will be different for the SOS diodes than for conventional devices.

SECTION 4
SECOND BREAKDOWN IN DIFFUSED DIODES AND TRANSISTORS

Two different thermal instability criteria have been observed for the SOS diodes described in Section 3: the temperature at the peak of the resistivity curve and the temperature where the reverse saturation current equals the avalanche current. These two mechanisms also appear to be dominant in diffused diodes and transistors, although they are often described in other terms, as noted in Section 2. Unfortunately, for diffused diodes and transistors, there is a distressing lack of good quantitative data on the breakdown temperatures versus doping density or resistivity due to the difficulty of determining the temperature in the interior of these devices. This difficulty in conventional devices is the reason that the SOS diodes with their exposed junctions and base regions have become so popular as test specimens.

About the best pieces of quantitative data, however, have been taken by Agatsuma et.al.[12], Melchior and Strutt[13], and Fleming[14]. The first two references claim agreement with the intrinsic temperature criterion (peak resistivity) while the latter opts for the reverse saturation current. In Reference 12, N^+NN^+ diodes (V_B from 40 to 100 V) were used with relatively long current pulses (50 cyc/sec repetitively swept). The authors say that the electric fields in the depletion region were orders of magnitude less than the avalanche threshold field. Hence, avalanche quenching could not be a triggering mechanism. In addition, they attempted to measure the temperature of their devices at breakdown using temperature-sensitive paints, and they show good correlation between their measured temperatures and the intrinsic temperatures versus base

resistivity. Similarly, in Reference 13, good agreement is obtained between the intrinsic temperature and the breakdown temperature for silicon MM1613 transistors. The breakdown temperatures were deduced from measurements made with different case temperatures and pulse widths from 0.1 to 2 msec. On the other hand, Fleming[14] calculated the temperature for a simple planar diode geometry as a function of input power and time and correlated the measured delay times with the time to reach the temperature for avalanche quenching as determined from the measured reverse saturation current. Note that the temperature for avalanche quenching is given as 650°K in this reference, whereas the peak resistivity for their 1 Ω-cm base material is about 520°K (Figure 2.1). Therefore, for the avalanche quenching argument to be valid, the bulk material would have to be over 130°K cooler than the junction. Such a difference is possible due to thermal diffusion, but it is by no means certain. Most other authors just speculate or assume that the triggering mechanism is one or the other of these two processes. A partial list of the papers that support the peak resistivity criterion is given in References 15 to 18, while those favoring the avalanche quenching are given in References 19 to 22. Domingos[23] reviews the SOS work and indicates that his experimental results are in general agreement with the Budenstein model, that is, both mechanisms occur. However, the tests were usually made with relatively long pulses (≈ms) so the results are not directly applicable to the time scale of our interest (≈ μsec).

Wunsch and Bell[24] performed a systematic study of the dependence of damage threshold on current pulse width. This was subsequently extended by Tasca.[25] Their results are in agreement with the thermal diffusion models discussed in Section 2. For very short pulses, thermal diffusion plays no role and the temperature increases linearly with time under electrical stress. When the pulse width becomes comparable to L^2/D, Where L is a characteristic dimension of the energy deposition region (e.g., depletion layer width), the peak temperature increases as the square

root of the time under stress. For even longer times, steady state heat flow to a heat sink (e.g., header, ambient air) is achieved and the peak temperature is dependent on the power level, independent of time.

In retrospect, it is probably not surprising that there is no clear-cut decision in favor of one of the two second breakdown triggering mechanisms. Even for the relatively simple geometries used in the SOS experiments, either instability could be dominant in a particular experiment depending on the resistivity of the base material, the current level, the pulse length, and probably the size of the devices and the methods of heat sinking. This uncertainty regarding the triggering instability for second breakdown results from the relatively equal magnitudes of the two critical temperatures at a given doping density in silicon. Moreover, this closeness of the temperatures seems to be a fairly general result for other resistivities as shown below.

In Figure 4.1, the temperature at the resistivity peak in Figure 2.1 is plotted versus doping density. Unfortunately, data are not available to define a similar curve based on the reverse saturation current. However, the closeness of the temperatures can be illustrated by the following calculations. From Figure 4.2 the temperature at which the reverse voltage goes to zero (i.e., reverse saturation current equals the total current) is 300°C for 1 mA current through the collector-base junction of a 2N1893 silicon transistor and 360°C for 10 mA of current. For comparison with the curve for the peak resistivity, these temperatures have been plotted in Figure 4.1 at the estimated collector doping density ($\approx 10^{15}/cm^3$). This density was obtained by using a nominal value of $BV_{CBO} = 120$ V for this device[26] and assuming an avalanche threshold field of 2×10^5 V/cm and a base doping much greater than the collector doping. It will be noted that the lower temperature (300°C) is less than 100°c above the peak resistivity curve. Moreover, if the temperature at the peak of the reverse

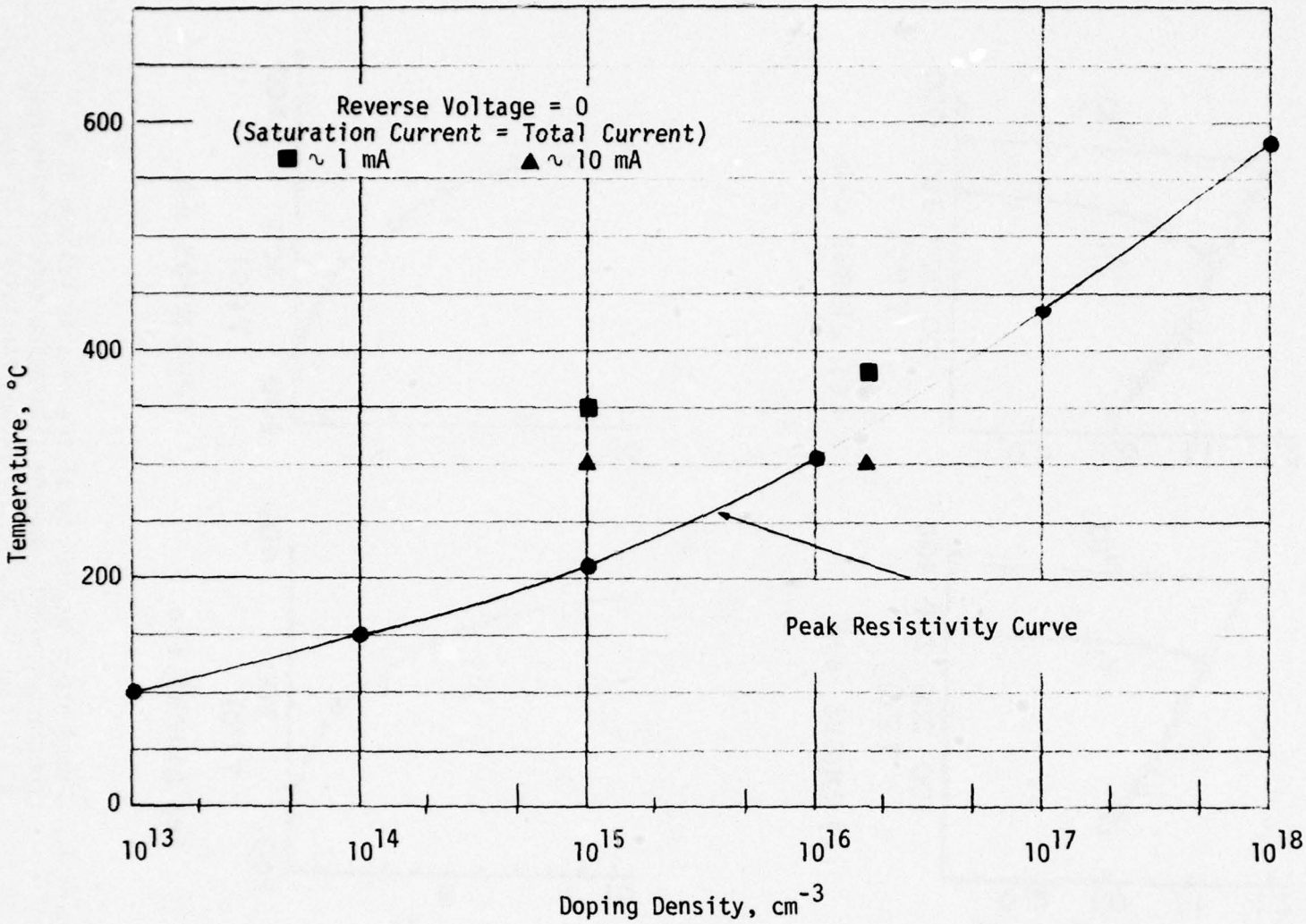


Figure 4.1 Comparison of Temperatures for peak resistivity and reverse saturation current = total current.

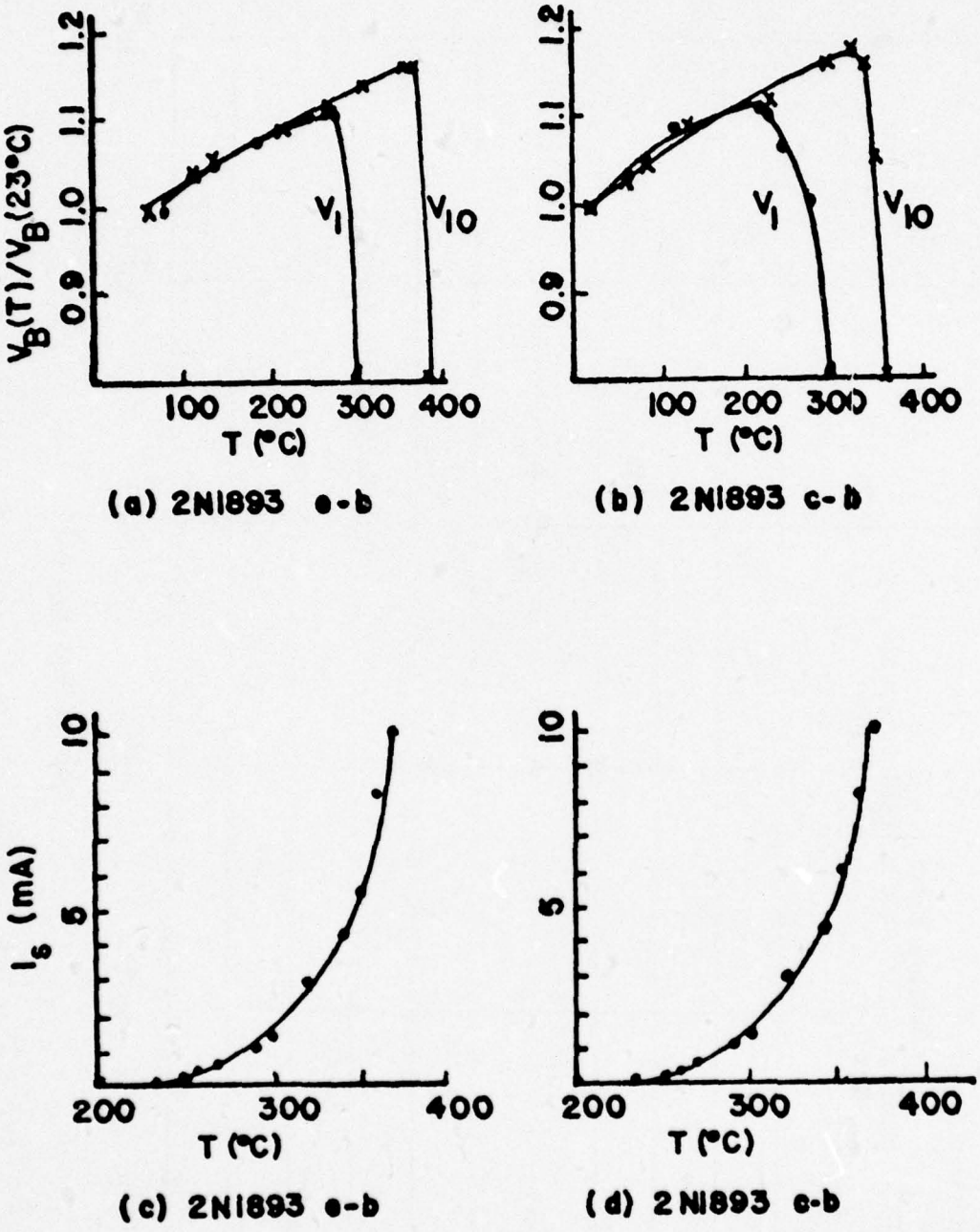


Figure 4.2 Temperature dependence of the reverse voltage at a constant current, and the saturation current measured at 5 volts in a 2N1893 silicon transistor. V_1 was measured at 1 mA reverse current, and V_{10} at 10 mA. (From Reference 7)

voltage curve (Figure 4.2) for 1 mA current had been used instead of the temperature at which $V_B(T)$ goes to zero, it would have fallen almost on the curve for the peak resistivity. Also, by using a nominal value of $BV_{BEO} = 7$ V in Figure 4.2, the base doping density (assuming a much larger emitter density) is approximately $1.7 \times 10^{16}/cm^3$. The two threshold temperatures (300°C for 1 mA and 380°C for 10 mA) are plotted in Figure 4.1 at this doping density. In this case, the lower temperature falls below the peak resistivity curve.

Based on the theoretical expression for the reverse saturation current, (Reference 27, Page 414) the critical temperature based on the reverse saturation current should follow the peak resistivity curve, as it appears to be doing in Figure 4.1.

$$I_o = A\, e\, n_i^2 \left(\frac{D_n}{p_{p_o} L_n} + \frac{D_p}{n_{n_o} L_p} \right)$$

In this expression, A is the junction area; e is the electronic charge; n_i is the intrinsic density; (D_n, D_p) and (L_n, L_p) are the diffusion lengths for the minority carriers (n and p) on the two sides of the junction; and p_{p_o} and n_{n_o} are the majority carrier densities on the two sides of the junction. At a given temperature, I_o increases with decreasing majority carrier density, that is, increasing resistivity, assuming the mobilities and lifetimes are not changed significantly. Therefore, for a given avalanche current, the temperature at which the reverse saturation current equals the avalanche current will be smaller at larger resistivities (smaller doping densities), which agrees with the curve for the peak resistivity.

From the above discussion, two conclusions can be drawn:

1. At the present time, it is very difficult to predict in general whether the triggering mechanism for thermal-mode second breakdown will be the peak resistivity or the reverse saturation current.
2. Two investigators who claim different instability temperature criteria for their triggering mechanisms could both be correct, depending on their test conditions and devices. However, the same temperature dependence might fit either criteria, within the accuracy of the data. Just because the data appears to fit one criterion does not necessarily rule out the other.

From an engineering standpoint, if both criteria yield essentially the same threshold curve for a given situation, it is immaterial which criterion is the triggering condition. The threshold value is the only important point. However, from the standpoint of predicting the change in the damage thresholds with variations in the device and test parameters, it is important to know the physics of each criterion and when they are dominant.

It is important to note that the resistivity peak is uniquely determined by the junction breakdown voltage (related to bulk resistivity). The diffusion current depends also on the minority carrier lifetime in the bulk semiconductor. The R-G current depends on the concentrations of deep-lying defect states in the depletion layer.

Up to this point, we have discussed the mechanisms of second breakdown in diodes and the application of the same mechanisms to planar

diffused transistors. We must now identify other factors that influence second breakdown in transistors. The extra features that must be considered are the influence of emitter injection on the collector current distribution and the lateral voltage drop produced by the flow of base current.

Emitter injection affects second breakdown in the collector-base junction in two ways:

1. Most of the emitter current passes through the collector junction, subtracting from the current that may be supplied by avalanching. Therefore, it reduces the temperature at which the diffusion and/or recombination-generation currents quench the avalanche and achieve the onset of a junction instability.
2. If the emitter current profile becomes filamentary because of a forward-biased junction instability, it produces a nonuniformity in the collector depletion-region energy deposition that partially overcomes the stabilizing effect of avalanche and collector resistivity.

In a transistor operating in the active region, the lateral base current produces a gradation in effective base-emitter bias, increasing from the center to the periphery. As a result there is a crowding of the emitter current density near the emitter periphery, which is reflected in the power deposition profile across the collector area. This inhomogeneity has the same type of effect on collector-base second breakdown as base-emitter junction filamentation.

In a transistor with open emitter lead, the lateral base current from collector-base avalanche breakdown produces a reverse bias across the base-emitter junction that increases from the center to the periphery.

At the sufficiently high current the periphery of the base-emitter junction can undergo avalanche breakdown, producing forward bias and injection in the center of the emitter-base junction. This produces an enhanced power density deposition in the center of the collector-base junction. The result is again to suppress the temperature at which the avalanche is quenched locally. This process can also exhibit a non-thermal prompt behavior, as discussed in Section 5.

In Reference 19 (Schroen), it was shown experimentally that collector-base junctions have lower damage thresholds, even with open emitters, than similarly-doped diode junctions. This breakdown of the emitter-base junction is apparently also a factor in current-mode second breakdown as discussed in Section 5.

The foregoing discussion of transistor base-collector second breakdown can also be applied directly to base-emitter second breakdown. The manifestations are modified somewhat because the emitter is much more heavily doped than the collector in a diffused transistor, resulting in a lower base-emitter breakdown voltage and a lower current gain in inverted operation.

SECTION 5
CURRENT MODE SECOND BREAKDOWN

The collector-emitter breakdown voltage, $B V_{CEO}$, on some devices undergoes at high currents a transition to a sustaining voltage well below the low-current avalanche breakdown voltage. Since the transition appears to occur as soon as the current exceeds a threshold value, and doesn't require the delay characteristic of thermal phenomena, it is called current-mode second breakdown. The following discussion explains the origin of this breakdown mechanism.

At low currents, the peak electric field in a junction occurs at the metallurgical junction plane. The net charge density in the depletion region is essentially just the ionized doping density. The junction field decreases toward zero at the edges of the depletion region at a rate proportional to the ionized doping density. However, at sufficiently high current densities, the mobile carrier densities in the depletion region are no longer negligible compared to the doping density. As a result, the electric field profile can be altered considerably as a function of current density.

This process can be illustrated by considering a typical epitaxial-transistor doping profile shown in Figure 5.1. Figure 5.2 illustrates the electric field is as shown in curve I, with slopes proportional to the net doping density in the base and epitaxial-collector sides of the junction. As the emitter current density is increased, the density of electrons passing through the junction becomes comparable with the epitaxial-collector dopant density. As shown in curve II, the slope

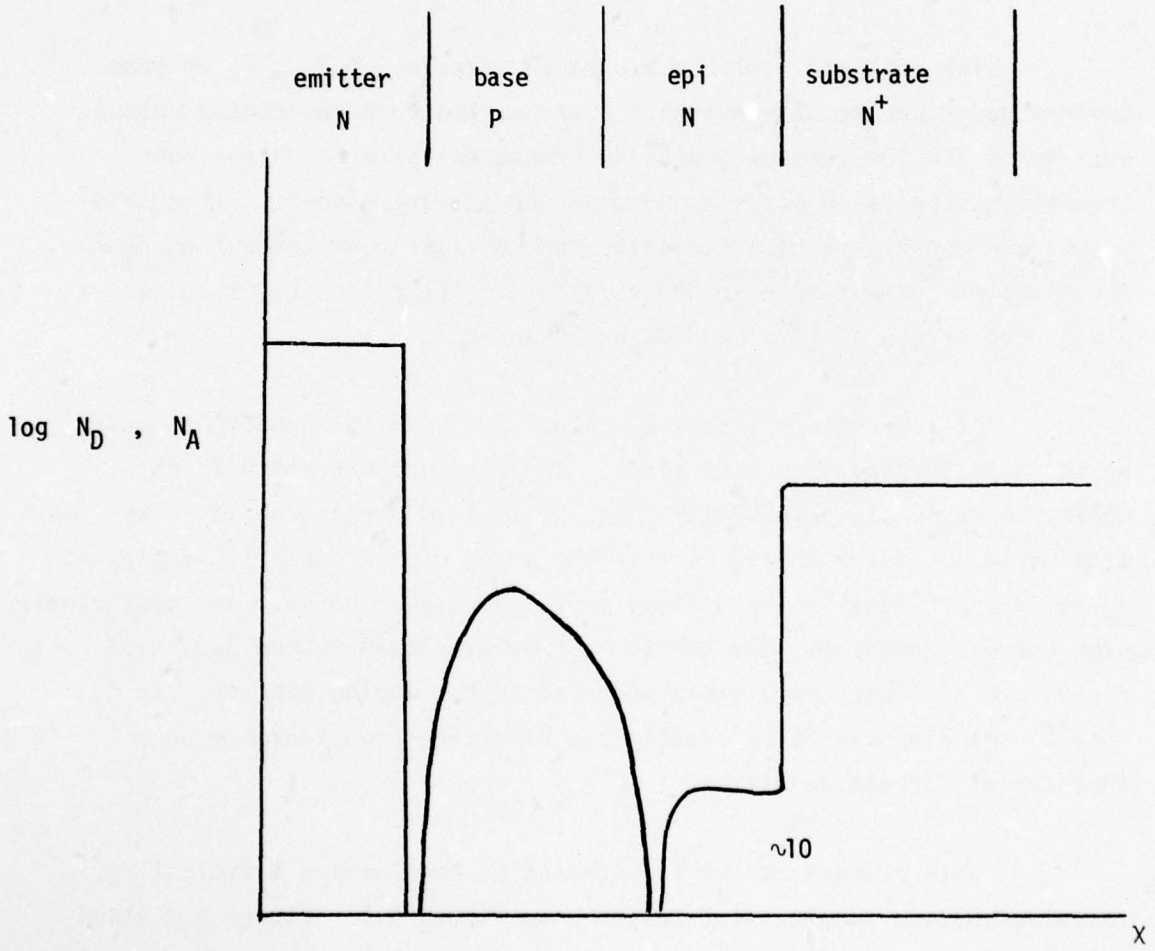
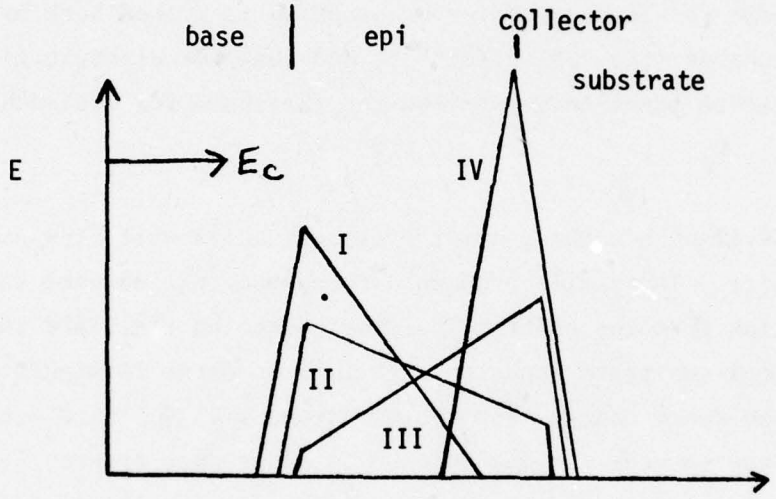


Figure 5.1 Epitaxial Transistor Profile



NOTE: assuming constant V_{CB} the area under each curve is equal

Figure 5.2 Electric Field Profile

on the base side steepens a little, but the slope on the collector side may decrease enough to extend the electric field to the heavily doped collector substrate. At higher current densities, the electron space charge can overcome the dopant density (curve III) and the electric field now peaks at the epi-substrate junction. At even higher current densities the effective edge of the base collector-junction is pushed back by the electron space charge (the Kirk effect[28]), and the peak electric field at the epi-substrate junction may exceed the threshold for avalanche multiplication , E_c .

Once avalanche occurs, a large flux of holes will flow back toward the emitter. These will produce a corresponding increase in electron injection from the emitter, further enhancing the field concentration at the epi-substrate junction. As long as there is significant current gain, the space charge from the electrons will dominate both the ionized donors and counter-flowing holes. This unstable process is limited by circuit parameters outside the base-collector junction. This avalanche process depends on the epitaxial structure. If the entire collector were of high resistivity material, electron injection would simply push the depletion layer into the collector without increasing the peak electric field.

A portion of this process can be explored by studying epitaxial diodes. Neudeck[29,30] has calculated the steady-state electric field distributions in planar P^+NN^+ diodes with various doping densities and N widths as a function of the current density. His results show that, as the current is increased, the junction voltage first increases as the electric field spreads out. This voltage increase continues until the depletion region reaches the N^+ substrate and the electric field is about constant across the N region. Since the electric field will not penetrate significantly into the N^+ region, the voltage ceases to increase with further current increase.

A sample of Neudeck's calculated electric field profiles[20] is shown in Figure 5.3. At even higher current densities, his calculations also exhibit the field concentration near the NN^+ junction discussed above, as shown in Figure 5.3. However, it is difficult to understand how the field in the remainder of the N region can decrease, because in a diode there is no externally injected electron flux. The electrons created by avalanching in the NN^+ region will move into the N^+ region, and only the holes will move across the N region. These holes should actually augment the donor charge density. This argument implies that the almost uniform electric field shown at 1.75×10^3 A/cm^2 in Figure 5.3, is essentially the limiting case in diodes and that the turnover to lower voltage at higher currents should occur only in transistors. We are not aware of any experimental data on P^+NN^+ diodes exhibiting prompt, current-mode second breakdown. There are data and calculations that exhibit second breakdown type behavior on N^+NN^+ diodes.[31] In this case the drift of holes to the left in Figure 5.3 causes electron injection, and the high-current behavior is very similar to a transistor.[31]

In epitaxial transistors the high-injection modulation of the effective BV_{CEO} can produce an oscillatory behavior.[32] In effect, the regenerative process of avalanche near the epi-substrate junction, enhancing the emitter current, which enhances the avalanching field concentration produces a rapid rise in current through the transistor. The current rise decreases the V_{CE} due to lead series impedance (e.g., inductance). Therefore, the current is temporarily supplied by stray capacitance, which discharges below the sustaining voltage, extinguishing the avalanche. After the capacitance is recharged through the leads, the injection and avalanche recur.

Another type of current-mode second breakdown in transistors is exhibited in the BV_{CBO} mode. With the emitter open and the collector

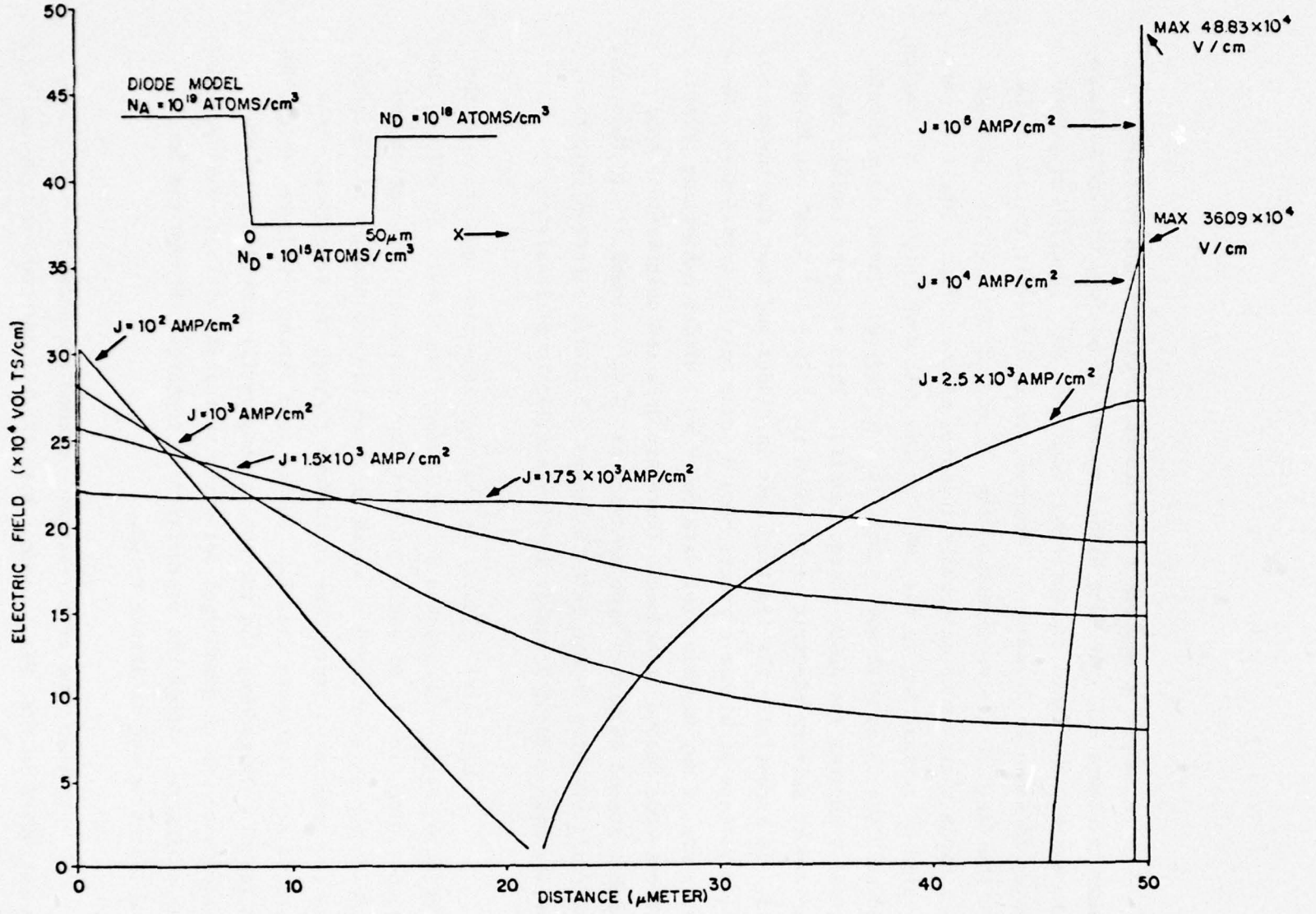


Figure 5.3 E vs x for reverse biased $P^+N^-N^+$ diode, X_o = 50 μ (From Reference 29)

base junction in avalanche, there is a considerable lateral voltage drop acorss the base sheet resistance between collector and emitter. When this voltage drop exceeds BV_{EBO} the emitter-base junction will break down at the periphery, providing emitter injection in the middle. This injection enhances the collector current, leading to enhanced avalanche currents, i.e., a runaway mode. This mechanism has explained superlinear ionization induced photocurrents,[33,34] in which the initiating base current is provided by ionization rather than avalanching.

The development of these unstable conditions is purely electronic and thus is relatively rapid, as compared to the thermal mode instabilities which depend on heating and thermal diffusion. For a saturation carrier velocity of about 10^7 cm/sec and a width for an epitaxial region of 10 μm , the characteristic time for the instability to develop is about 0.1 nsec.

SECTION 6
SUMMARY

The mechanisms which play major roles in thermal and current-mode, second breakdown and junction burnout, have probably all been identified and are fairly well understood. In thermal-mode second breakdown, high-current filamentary tracks through the junction are initiated by a combination of two instabilities, avalanche quenching and resistivity peak, when the local temperatures reach the critical temperatures for these instabilities. Current-mode second breakdown is initiated by purely electronic processes (avalanche injection at high current densities in epitaxial structures when the high field region of the collector-base junction transfers to the collector-substrate junction, and breakdown of the emitter-base junction due to lateral biasing by the base current). Current-mode second breakdown also develops filamentary current channels which can then cause failure by overheating.

Although all the fundamental processes have probably been identified, there is inadequate knowledge on the quantitative application of these processes for predicting the ranges of device damage thresholds and the scaling of these thresholds with electrical stress parameters. Competition between power deposition and thermal diffusion, complementarity between avalanche quenching and bulk resistivity turnover, and the additive effects of minority-carrier diffusion and recombination-generation currents will scale differently for various device profiles and electrical pulse widths. The importance of structural defects in the device also varies greatly between different mechanisms.

The implications of the fundamental mechanisms for practical device behavior have not been completely worked out. In particular, it should now be possible to define regions in a parameter space (device and electrical-stress parameters) in which individual mechanisms control the onset of second breakdown and permanent damage. For each region the controlling parameters should be identified and their credible limits for devices not subjected to special burnout controls established. Controls to limit the damage threshold should then be formulated.

Lower limits to the energy required to burn out a device can be established by adding the minimum energy to achieve second breakdown* to the energy required to heat at least one of the resulting filaments to a damage temperature. The lower limit energy for each portion is determined from the minimum temperature change required to achieve the instability or damage, the minimum volume in which the temperature change must occur, and the specific heat of the semiconductor.

The advantage of separating the energy into two phases is that upon the onset of second breakdown the stabilizing factors tend to make the current flow uniformly over the junction area. Therefore, the minimum volume to be heated tends to encompass the entire junction area. Above the onset of second breakdown, the current flow will be filamentary, and the minimum volume is determined by the electro-thermal dynamics of each filament and boundary conditions that determine the minimum number of filaments.

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* We will continue to use the theoretically oriented definition of the onset of second breakdown as the occurrence of an instability.

If there were no forces to produce nonuniformities in current density across a junction, the minimum energy to achieve second breakdown could be calculated by identifying the lowest instability temperature (peak resistivity, avalanche quenching by diffusion, or R-G current) and multiplying the temperature change by the specific heat, the junction area, and an effective junction thickness determined by the electric field profile perpendicular to the junction convoluted with thermal diffusion. The dependence of minimum energy on electrical pulse width would come from thermal diffusion and from a possible shift in lowest instability temperature in going to higher current densities as the pulse width is shortened. Current-mode second breakdown and true Zener junctions are defined to have a zero minimum energy.

The sensitivity of the dependence of the lowest critical temperature on fluctuations in device structure parameters and the ease of measurability of these parameters is influenced strongly by the process which is responsible for triggering an instability. If the resistivity peak is the trigger, the critical temperature is a function of maximum bulk resistivity only, which is measured by the junction breakdown voltage. If reverse diffusion current is responsible for avalanche quenching, the minority carrier concentration (proportional to resistivity) and minority carrier diffusion length are relevant parameters. The diffusion length at ambient temperatures can be determined from response-time measurements, but some assumptions are required to extrapolate the results to temperatures of interest. If R-G current can quench the avalanche, its magnitude also depends on the concentrations of recombination centers in the depletion layer with energy near the intrinsic Fermi level. Control of the parameters controlling the R-G current may require measurements of the reverse saturation current at elevated temperatures.

The foregoing analysis can be based on a one-dimensional description of the electric field and temperature profile. If the time to achieve second breakdown is long compared to minority carrier lifetime in the device (ranging from 10^{-8} to 10^{-6} sec in different devices), the analysis can use a quasi-state version of the electron, hole, and electric-field continuity equations. If fast pulses are to be considered, the time-dependent continuity equations for electrons, holes, and electric-field are required.

In practical devices there are forces that tend to make the current flow across a junction nonuniform, including dopant nonuniformities, local defects, emitter-current crowding, etc. Even though there are also stabilizing factors (temperature dependence of avalanche field, extrinsic resistivity) there will still be some nonuniformity in current flow below the onset of second breakdown. As a result the average temperature rise over the junction area will be less than that required to bring its hottest spot to the onset of an instability.

As Budenstein's work[7] has demonstrated, the onset of an instability at one point, on the junction doesn't necessarily produce any dramatic changes in the device voltage, nor does it automatically lead to a thermal runaway. At least in some device structures, the volume in which the current flow is unstable must grow by heating nearby bulk material past the resistivity peak before permanent damage, or even a dramatic voltage drop (e.g., that associated with an experimental characterization of second breakdown) occurs. The analysis of the minimum energy required during this phase is at least two-dimensional by the nature of the instability. The lateral dimensions of the filament are determined in part by thermal diffusion, and in part by electrical factors (e.g., electric field is proportional to current density). There are competing factors in the time dependence. Long current pulses produce larger

filaments by thermal diffusion. Short higher-current pulses produce a larger number of filaments because of transverse voltage drops.

One way of avoiding the complexities in the two-dimensional analysis of current filaments is to establish the safe-design maximum energy at the minimum energy value to achieve the onset of second breakdown. This does not eliminate the need to assess the impact of inhomogeneous forces (those that promote nonuniform flow) on the minimum energy for second breakdown.

The variety of instability triggering mechanisms discussed in previous sections of this report and the wide spread in reported experimental results force us to conclude that there are various classes of device structures in which the instability triggering mechanism is different. The characteristics of each class must be defined in such a way that each device type can be assigned to a class. For each class the critical parameters that determine the minimum damage energy must be identified. Where needed, controls for the critical parameters must be developed and standardized.

As described above the required mechanisms knowledge is designed particularly for application to Hardness Assurance. The concept of a (pulse-width dependent) minimum damage energy, which equates to a definition of a high-confidence safe operating region, can be used to control the management interface between device procurement and system design. The quantitative understanding of the relationship between measurable device parameters and minimum damage energy leads directly to procurement specifications and guidelines for system design.

The same knowledge can be used to design devices with higher damage thresholds (i.e., harder parts). It can also be used to

characterize the typical device (e.g., mean and standard deviation of damage stress) but this information is also accessible by performing small-sample tests. The mechanisms knowledge assists in scaling test results to different conditions (e.g., pulse shape, temperature, electrical-ionization synergisms). But its most vital role is in extending the results of limited tests to a high-confidence design guideline and device quality controls.

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		Return 3